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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/542,986	07/21/2005	Gunnar Normark	1554-1005	5635
<small>465</small> YOUNG & THOMPSON 209 Madison Street Suite 500 ALEXANDRIA, VA 22314			<small>7590</small> EXAMINER GEIB, BENJAMIN P	
			ART UNIT 2181	PAPER NUMBER
			MAIL DATE 02/18/2009	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

10/542,986

**Applicant(s)**

NORMARK ET AL.

**Examiner**

BENJAMIN P. GEIB

**Art Unit**

2181

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 November 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 10-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 10-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 July 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)  
Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 10-12, 15, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Hoof et al., U.S. Patent No. 7,080,238 (Hereinafter Van Hoof).

3. Referring to claim 10, Van Hoof has taught a method in a processor, in which data is processed in a pipelined manner [column 3, lines 31-38], the data being included in a plurality of contexts, comprising a first context (3) [column 3, lines 49-59], each context passing a plurality of consecutive stages (2a-2f), in addition to which a plurality of operations is adapted to be executed on the contexts, the method comprising executing an initial operation step (6a) of a first operation on the first context (3), and subsequently commencing an execution on the first context of an initial operation step (7a) of a second operation before an execution of the first context (3) of a following operation step (6b) of the first operation is completed [Since instructions are processed in a pipeline manner, an operation may enter the pipeline while a previously dispatched operation is still within the pipeline; column 3, line 60 – column 4, line 4], characterized in that,

- at each clock cycle of the processor, the first context (3) is received at one of the stages from the preceding stage, the first context is unconditionally moved to a next stage, [See Fig. 3; column 4, lines 58-60]
- the initial operation step (6a) of the first operation is executed on the first context (3) at a first stage (2a) [the first stage sub-processor executes the initial operation step on the first context; column 3, line 60 - column 4, line 4; Fig. 2],

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- the following operation step (6b) of the first operation is executed of the first context (3) at a second stage (2b) *[the second stage sub-processor executes the following operation step on the first context; column 3, line 60 - column 4, line 4; Fig. 2], and*
  - the initial operation step (7a) of the second operation is executed on the first context at the second stage (2b) *[the first stage sub-processor executes the initial operation step of a different operation on the first context; column 3, line 60 - column 4, line 4; Fig. 2].*
4. Referring to claim 11, Van Hoof has taught a method according to claim 10, comprising commencing at the first stage (2a) an execution of the initial operation step (6a) of the first operation on a second context before the execution on the first context (3) of the following operation step (6b) of the first operation is completed *[FIG. 2; column 4, lines 25-37].*
5. Referring to claim 12, Van Hoof has taught a method according to claim 10, comprising receiving at the second stage a result (R6a) of an execution of the initial operation step (6a) of the first operation *[FIG. 2; column 4, lines 30-35].*
6. Referring to claim 15, Van Hoof has taught a method according to claim 10, whereby the processor is arranged so that the following operation step (6b) of the first operation is presented to a programmer as being executed at the first stage (2a) *[The operation step/stages are not seen by the programmer and are, therefore, presented similarly; column 3, lines 31-38].*
7. Referring to claim 16, Van Hoof has taught a method according to claim 10, wherein the first operation comprises a partial operation of executing (6c1) an instruction and a partial operation of writing (6c2) a result of the said instruction execution into a destination in a register, and the second operation comprises the partial operation of fetching (7a2 1, 7a22) an operand, the method comprising (a) determining if a position in the register, from which the operand is to be fetched (7a 1 1, 7a22) in the second operation, is identical with the destination of the partial operation, of the first operation, of writing (6c2) a result, and (b) if the result of the determination in step (a) is negative, fetching (7a21) the operand from the register, and (c) if the result of the determining in step (a) is positive, fetching (7a22) the result of the said instruction execution *[column 4, lines 25-43].*

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hoof in view of Wallace et al., "Threaded Multiple Path Execution" (Hereinafter Wallace).

10. Referring to claim 13, Van Hoof has taught a method according to claim 10, whereby at least one of the operation steps of the second operation comprises at least two alternative execution paths [*Van Hoof; conditional branch instruction; column 5, lines 19-26*].

Van Hoof has not explicitly taught at least two of the alternative execution paths of the operation step are executed.

Wallace has taught wherein at least two alternative execution paths of an operation step are executed [*Wallace; section 3*].

At the time the invention was made, it would have been obvious to modify the method of Van Hoof to include executing at least two of the alternative execution paths of the operation step.

The motivation for doing so would have been that the probability of executing on the right path is increased [*Wallace; section 3*], thereby increasing performance as would be understood by one of ordinary skill in the art.

11. Referring to claim 14, Van Hoof has taught a method according to claim 13, further comprising: obtaining results (R7b1, R7b2) of at least two of the executions of the alternative execution paths, and determining, based on a result (R6) of an execution of an operation step of an operation initiated before the initiation of the second operation, which one of the results (R7b1, R7b2), of the execution of the alternative execution paths, an execution of an operation step of the second operation, following said operation step comprising at least two alternative execution paths, is to be based on [*Wallace; page 4, right column, 7<sup>th</sup> and 8<sup>th</sup> paragraphs*].

***Response to Arguments***

12. Applicant's arguments filed 11/28/2008 have been fully considered but they are not persuasive.
13. Applicant argues the novelty/rejection of the claims, in substance that:

a) "Van Hoof does not disclose 'the following operation step (6b) of the first operation is **executed of the first context (3) at a second stage (2b)**'" (1<sup>st</sup> paragraph, page 8)

b) "The prior art fails to disclose at each clock cycle, the first context is unconditionally moved to a next stage" (2nd paragraph, page 8)

c) "Van Hoof cannot disclose 'the processor is arranged so that the following operation step (6b) of the first operation is presented to a programmer as being executed at the first stage (2a),' as in claim 15" (2nd full paragraph, page 9)

14. These arguments are not found persuasive for the following reasons.

15. Regarding argument a), the applicant argues that Van Hoof has not taught the cited limitation because all the operation steps of an operation are performed within a single stage. However, the fact that Van Hoof has taught that all the steps of a single instruction may be performed with a single sub-processor does not prevent Van Hoof from teaching "the following operation step (6b) of the first operation is executed of the first context (3) at a second stage (2b)" as claimed. As previously noted, the second stage sub-processor executes the following operation step on the first context (column 3, line 60 - column 4, line 4) and, therefore, Van Hoof has taught "the following operation step (6b) of the first operation is executed of the first context (3) at a second stage (2b)" as claimed. It appears to the examiner that the applicant is reading this limitation too narrowly and it is suggested that the claims be amended to more particularly indicate the "operation step" and "operation" being performed.

16. Regarding argument b), Van Hoof has taught that "the sub-processor 40 preferably processes each context for an allotted context processing time, such as, for example, one clock cycle, and performs a context switch for processing a next available context in the context pool after the allotted context processing time has expired." Column 5, lines 9-14. Therefore, Van Hoof has taught that every clock cycle a context is unconditionally switched. This act of unconditionally switching contexts moves the context to the next stage in the pipeline. Therefore, Van Hoof has taught at each clock cycle "the first context is unconditionally moved to a next stage."

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17. Regarding argument c), as noted above the operation step/stages of a sub-processor are not seen by the programmer because they are executed within a clock cycle (column 5, lines 9-14).

Therefore, the following operation step of the first operation is presented to a programmer as being executed at the first stage

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Benjamin P Geib  
Examiner  
Art Unit 2181

/Benjamin P Geib/  
Examiner, Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181